Sharad Malik

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Contact Information

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Research Interests

Design methodology for computing systems; functional and security verification of digital systems.

Education

- Ph.D. in Computer Science, Univ. of California, Berkeley, December 1990
- M. S. in Computer Science, Univ. of California, Berkeley, May 1987
- Bachelor of Technology in Electrical Engineering, Indian Institute of Technology, New Delhi, May 1985

Professional Experience

Princeton University Department of Electrical and Computer Engineering

- George Van Ness Lothrop Professor of Engineering: September 2005 – present
  - July 2012-June 2021: Chair, Department of Electrical and Computer Engineering
  - December 2012-July 2016: Associate Director, Center for Future Architectures Research (C-FAR) (www.futurearchs.org)
  - November 2009-November 2012: Director, Gigascale Systems Research Center (GSRC)
  - September 2006-August 2011: Director, Keller Center for Innovation in Engineering Education (kellercenter.princeton.edu)
- Professor - July 1999 to August 2005
- Associate Professor - July 1996 to June 1999
- Assistant Professor - February 1991 to June 1996

Current Board Assignments

- Board of Directors, Info Edge, India
- Academic Advisory Board, Plaksha University, India
- Academic Advisory Council, Ashoka University, India

University of California, Berkeley, Computer Science Department

- Post-Graduate Researcher - May 1986 to December 1990
- Teaching Assistant - August 1985 to May 1986

AT&T Bell Labs, Murray Hill, NJ

Summer Research Intern - May 1989 to August 1989

Awards and Honors

- "Leveraging Processor Modeling and Verification for General Hardware Modules" (co-authored with Yue Xing, Huaixi Lu, and Aarti Gupta); Best Paper Award, Design and Tools Track; Design, Automation & Test in Europe Conference (DATE), 2021
- "Instruction-Level Abstraction (ILA): A Uniform Specification for System-on-Chip (SoC) Verification," (co-authored with Bo-Yuan Huang, Hongce Zhang, Pramod Subramanyan, Yakir Vizel, and Aarti Gupta), Best Paper Award, ACM Transactions on Design Automation of Electronic Systems (TODAES), 2020
- University of California Berkeley, Department of Electrical Engineering and Computer Science, Distinguished Alumni Award in Electrical Engineering, 2019
- Intel Corporate Research Council Outstanding Researcher Award (Security and Software Sector), 2018
- IEEE CEDA A. Richard Newton Technical Impact Award in Electronic Design Automation, 2017
- "Evaluating the Security of Logic Encryption Algorithms," (co-authored with P. Subramanyan and S. Ray), Best Student Paper Award, IEEE International Symposium on Hardware Oriented Security and Trust (HOST), 2015
- "On computing minimal independent support and its applications to sampling and counting," (co-authored with A. Irvii, K. Meel and M. Vardi), Best Student Paper Award, 21st International Conference on Principles and Practice of Constraint Programming (CP), 2015
- "Hardware Trojan detection for gate-level ICs using signal correlation based clustering," (co-authored with B. Cakir), Best Paper Award in Application Design, Design Automation and Test in Europe (DATE), 2015
- ACM Fellow 2015
- The IEEE/ACM Design Automation Conference 50th Anniversary Most Cited Paper Award: (with M. W. Moskewicz, C. F. Madigan, Y. Zhao and L. Zhang) For publishing the most cited paper in DAC's 50 year history, 2013
- The IEEE/ACM Design Automation Conference 50th Anniversary Award: For the Author with the Second Most Citations from DAC Publications in DAC's 50-year history, 2013
- The IEEE/ACM Design Automation Conference 50th Anniversary Prolific Author Award For publishing 20 or more papers at the Design Automation Conference, 2013
- "Accelerating Boolean Satisfiability with Configurable Hardware," (co-authored with P. Zhong, M. Martonosi and P. Ashar), selected for inclusion in "Significant Contributions from 20 Years of the International IEEE Symposium on Field-Programmable Custom Computing Machines (1993-2013)," 2013
- "Efficient Conflict-Driven Learning in a Boolean Satisfiability Solver," (co-authored with L. Zhang, M. Moskewicz and C. Madigan), IEEE/ACM International Conference on Computer-Aided Design, Ten Year Retrospective Most Influential Paper Award, 2011
- Princeton University President's Award for Distinguished Teaching, 2009
- Distinguished Alumni Award, Indian Institute of Technology Delhi, 2009
- Computer-Aided Verification (CAV) Award for fundamental contributions to the development of high-performance Boolean satisfiability solvers, 2009
- IBM Faculty Award, 2007, 2006, 1991
- Princeton University, School of Engineering and Applied Sciences, Distinguished Teacher Award, 2005.

- "Validating SAT Solvers Using an Independent Resolution-Based Checker: Practical Implementations and Other Applications," (co-authored with L. Zhang), Best Paper Award, IEEE/ACM Design Automation and Test in Europe (DATE), 2003.
- "Power Analysis of Embedded Software: A First Step Towards Software Power Minimization," (co-authored with V. Tiwari and A. Wolfe), selected to be included in "The Best of ICCAD – 20 Years of Excellence in Computer-Aided Design," 2003
- IEEE Fellow, 2002
- "Using register-transfer paths in code generation for heterogeneous memory-register architectures", (with G. Araujo and M. T-C. Lee), Best Paper Award, IEEE/ACM Design Automation Conference June 1996.
- NSF Young Investigator Award, May 1994
- Rheinstein Faculty Award, School of Engineering and Applied Sciences, Princeton University, May 1994
- Engineering Council Excellence in Teaching Award, Princeton University, January 1996, May 1994, May 1993
- Walter C. Johnson Prize for Teaching Excellence, Dept. of Electrical Engineering, Princeton University, May 1993
- NSF Research Initiation Award, August 1992
- Best Paper Award, IEEE International Conference on Computer Design, 1992
- "Delay Computation in Combinational Logic Circuits: Theory and Algorithms," (co-authored with K. Keutzer and S. Devadas), Distinguished Paper Citation, International Conference on Computer-Aided Design, 1991
- University of California Regents Fellowship, 1985 and 1986
- President of India's Gold Medal, IIT Delhi, 1985 for undergraduate academic excellence

Patents and Inventions

- US Patent 7,418,369, August 26, 2008: "Method and System for Efficient Implementation of Boolean Satisfiability"
- US Patent 6,961,916, November 1, 2005: "Placement method for integrated circuit design using topo-clustering"
- US Patent 6,874,135, March 29, 2005: "Method for design validation using retiming"
- US Patent 6,651,234, November 18, 2003: "Partition based decision heuristics for SAT and image computation using SAT and BDDs"
- US Patent 6,449,756, September 10, 2002: "Method for accurate and efficient updates of timing information in logic synthesis, placement and routing for integrated circuit design"
- US Patent 6,442,743, August 27, 2002: "Placement method for integrated circuit design using topo-clustering"
- US Patent 6,367,051, April 2, 2002: "System and method for concurrent buffer insertion and placement of logic gates"
- US Patent 6,286,128, September 4, 2001: "Method for design optimization using logical and physical information"
- US Patent 6,247,164, June 12, 2001: "Configurable hardware system implementing Boolean Satisfiability and method thereof"
- US Patent 6,192,508, Feb 20, 2001: "Method for Logic Optimization for Improving Timing and Congestion During Placement in Integrated Circuit Design"
- US Patent 5,937,183, August 10, 1999: "Enhanced Binary Decision Diagram Based Functional Simulation"
- US Patent 5,841,673, November 24, 1998: "System and method for processing graphic delay data of logic circuit to reduce topological redundancy"
- US Patent 6,038,392, May 27, 1998: "Implementation of Boolean satisfiability with non-chronological backtracking in reconfigurable hardware"

- US Patent 6,035,109, April 22, 1997: “Method for using complete-1-distinguishability for FSM equivalence checking”
- US Patent 5,522,063, May 28, 1996: “Method of Finding Minimum Cost Feedback Vertex Sets for a Graph for Partial Scan Testing without Exhaustive Cycle Enumeration”
- US Patent 5,457,638, October 10, 1995: “Timing Analysis of VLSI Circuits”
- US Patent 5,448,497, September 5, 1995: “Exploiting multi-cycle false paths in the performance optimization of sequential circuits”

Program Committee Assignments

- Academic Co-Chair of the EDA event at SAT 2021
- Workshop on Resiliency of Embedded Electronic Systems (REES): 2015
- International Conference on Runtime Verification (RV): 2012
- Haifa Verification Conference (HVC): 2006, 2007, 2008, 2009 Awards Committee Chair
- International Conference on Computer-Aided Verification: 2005, 2008 (co-chair)
- The International Conference on Theory and Applications of Satisfiability Testing (SAT): 2003, 2004, 2005, 2006, 2015
- International Conference on Embedded and Hybrid Systems: 2004
- Design Automation and Test in Europe (DATE): 2004
- Workshop on Bounded Model Checking: 2003, 2004, 2005
- Workshop on Parallel and Distributed Model Checking: 2003, 2004
- The ACM SIGBED International Conference on Embedded Software (EMSOFT): 2003
- IEEE/ACM Design Automation Conference: 1994, 1995, 1996, 1997, 1998, 1999. Program Co-Chair, DAC 2000 and DAC 2001. Panels Chair 2002. General Chair 2004.
- Constraints in Formal Verification: 2002
- IEEE International Conference on Computer-Aided Design: 1992, 1993, 1994, 1995 (Chair, sub-committee on timing analysis and optimization, 1994, 1995)
- Asia-Pacific Design Automation Conference: 1997, 1998
- IEEE/ACM International Symposium on Low Power Electronics and Design: 1997, 1999, 2000
- ACM International Workshop on Logic Synthesis: 1991, 1993, 1997 (Technical Program Chair), 1998
- ACM International Workshop on Timing Issues in the Specification, Design and Synthesis of Digital Systems: 1992 (Workshop chair), 1993, 1995, 1997
- ACM SIGPLAN Workshop on Languages, Compilers and Tools for Embedded Systems: 2000.
- Asynchronous Design Symposium: 2000
- European Design and Test Conference: 1994, 1995
- IEEE International Conference on Computer Design: 1992, 1994
- International Workshop on Low Power Design: 1995
- IEEE International Conference on VLSI Design: 1992

Editorial Boards

- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Editor-at-Large, February 2020 - present
- Foundations and Trends in Electronic Design Automation, NOW Publishers, Editor-in-Chief: 2005-2011
- IEEE Transactions on VLSI Systems: 2007-2009
- ACM Transactions on Design Automation of Electronic Systems: 2005-2008
- Formal Methods in System Design, Springer-Verlag: 2005 - present
- IEEE Design and Test: 2001 – 2008

    - Guest Editor: Special Issue on "Exploring Synergies for Design Verification," November-December 2004
- Journal on Satisfiability, Boolean Modeling and Computation (IOS Press): 2003-present
- Design Automation of Embedded Systems, Kluwer Academic Publishers: 1995 - present
- Journal of VLSI Signal Processing, Kluwer Academic Publishers: 1996 - 2005
    - Guest Editor: Journal of VLSI Signal Processing, Special Issue on Asynchronous Circuits, Kluwer Academic Publishers, October 1993.

Invited Presentations

Talks

- "Academic Job Search: A Chair's Perspective," JOBS Workshop at MICRO Conference 2022, October 1, 2022
- "Hardware-Software Interface Specification for Verification in Accelerator-Rich Platforms," Keynote Talk, Latte 21 Workshop at ASPLOS, April 15, 2021.
- "Formal Methods in Systems-on-Chip (SoC) Security Verification," Keynote Talk, IEEE Asian Hardware Oriented Security and Trust Symposium (AsianHOST), December 16, 2020
- "Instruction-Level Abstraction (ILA):A Uniform Specification for System-on-Chip (SoC) Verification," Keynote Talk, Jasper Users Group Conference, October 11, 2018
- "Specification and Modeling for Systems-on-Chip Security Verification," Invited Talk, Design Automation Conference, June 6-8, 2016.
- "Detecting Hardware Trojans: A Tale of Two Techniques," Invited Talk, Formal Methods in Computer-Aided Design, September 29, 2015.
- "Boolean Satisfiability: From Theoretical Hardness to Practical Success," ECE Distinguished Lecture, Boston University, January 29, 2014
- "Boolean Satisfiability: From Theoretical Hardness to Practical Success," Weber Lecture, NYU Poly, October 31, 2013
- "Verification of Computer Switching Networks: An Overview," Invited Talk, Tenth International Symposium on Automated Technology for Verification and Analysis, ATVA 2012
- "Runtime Verification: A Computer Architecture Perspective," Invited Talk, International Conference on Runtime Verification, 2011, San Francisco.
- "Boolean Satisfiability Solvers and Extensions," Invited Talk, Advanced Study Institute of the NATO Science for Peace and Security Programme, Tools for Analysis and Verification of Software Safety and Security, August 2011, Marktoberdorf, Germany.
- "Boolean Satisfiability: From Theoretical Hardness to Practical Success," Invited Seminar, Summer Research Institute, School of Computer and Communication Sciences, École Polytechnique Fédérale de Lausanne (EPFL), June 20, 2011
- "Design Debugging using Boolean Satisfiability," Invited Talk, First International SAT/SMT Solver Summer School 2011, MIT, June 2011
- "Managing State Explosion through Runtime Verification," Hardware Verification Workshop (in association with Computer-Aided Verification), July 15, 2010, Edinburgh.
- "Design Methodology and Verification in the Context of Third Party IP," DARPA Trust Third Party IP Workshop, November 20, 2008
- "SAT and QBF Solvers," NSF Workshop on Symbolic Computation for Constraint Satisfaction Problems, November 14, 2008
- "Hardware Verification: Techniques, Methodology and Solutions,"
    - Keynote Talk, Tools and Algorithms for the Construction and Analysis of Systems (TACAS), April 4, 2008, Budapest.
    - Invited Seminar, Cornell University, May 19, 2008.

- "SAT Solvers: Efficient Implementations," NSA DoD SAT Workshop, Baltimore, MD, March 3, 2008
- "Verification Driven Formal Architecture and Microarchitecture Modeling,"
  - IBM Research, Yorktown Heights, December 12, 2008.
  - Intel Annual Symposium, Haifa, July 10, 2007.
- "Optimization and Relaxation in SAT Search," Workshop on Satisfiability Solvers and Program Verification, Seattle, August 11th 2006.
- "A Case for the Runtime Validation of Hardware," Keynote Speaker, IBM Verification Conference, Haifa, November 13th 2005.
- "Experiences with QBF Solvers," Workshop on Bounded Model Checking, Edinburgh, July 11th 2005.
- "The Quest for Efficient SAT Solvers," Carnegie-Mellon University, School of Computer Science, Distinguished Lecture Series, The Gaschnig/Oakley Memorial Lecture, April 22, 2004.
- "Gigascale Silicon Design: Challenges and Opportunities," Keynote Speaker, Intel Design and Test Conference, Portland, July 29th, 2003.
- "Embedded Software Implementation Tools for Fully Programmable Application-Specific Systems," Workshop on Embedded Software (EMSOFT), Grenoble, October 9th, 2002.
- "The Quest for Efficient SAT Solvers," Computer-Aided Verification/Conference on Automated Deduction (Joint Invited Talk), Copenhagen, July 29th, 2002
- "Chaff: Engineering an Efficient SAT Solver."
  - Intel Logic Verification Symposium, 24th July, 2001, Weizmann Institute of Science, Israel.
  - Compaq Corp., Shrewsbury MA, 7th June, 2001
- "Enabling Fully Programmable Application Specific Solutions through MESCAL: Modern Embedded Systems, Compilers, Architectures and Languages."
  - Motorola Circuits Systems and Architectures Futures Forum, October 16, 2000
  - Enabling Technologies for System-on-Chip Development, Tampere University of Technology, November 15, 2000
- "Power Analysis for Embedded Software", Plenary Talk, PATMOS, September 1997
- "Worst-Case Static Timing Analysis - From Gates to Instructions", ACM/IEEE Workshop on Timing Issues in the Specification and Synthesis of Digital Systems, December 1997

Panels

- "Driving Architecture Specialization with Benchmarks for Emerging Applications," Panel Chair, Benchmarking Workshop, MICRO 2022 Conference, October 2, 2022
- "Uniform Processor/Accelerator/Device Specification for Simulation-Based/Formal Verification," DARPA ERI Summit ASIC Functional Verification Workshop, October 19, 2021
- "Dead or Alive? The Fate of Formal Methods in Securing "Everyday" SoCs," Design Automation Conference, July 23, 2020
- "ESL HW/SW Verification: A Reality Check," Panel Chair, ACM/IEEE Design Automation Conference, June 9, 2011
- National Academy of Engineering, Frontiers of Engineering Education, 2009 (Invited Participant)
- "Why Do We Still Have Bugs? Challenges from Design through System Software," P=ac^2 Workshop, IBM Research, March 31, 2008
- "Computer-Aided Verification in Many-Core Parallel Software," Workshop on Exploiting Concurrency Correctly and Efficiently, 2008

- "Building a Verification Test Plan – Trading Brute Force for Finesse," Panel Chair, IEEE/ACM Design Automation Conference, 2006
- "Embedded Systems Education," Panel Chair, IEEE/ACM Design Automation Conference, 2000
- "Compilers for Systems on a Chip," Panel Chair, IEEE International Conference on Computer Design, October 1997

Tutorials

- "Generalizing the ISA to the ILA: A Software/Hardware Interface for Accelerator-rich Platforms," (with Bo-Yuan Huang and Aarti Gupta), International Symposium on Computer Architecture, June 2022
- "Enabling FV and Simulation using Functional Specifications: The Open-Source ILA Methodology," (with C. Barrett and A. Gupta), Design Automation Conference, December 2021
- "CAD Techniques for Embedded Systems", IEEE VLSI Design, January 1999
- "Static Timing Analysis of Embedded Software", ACM Design Automation Conference, June 1997
- "Optimization Techniques for Low Power VLSI Circuits", IEEE International Conference on Computer-Aided Design, November 1995
- "Register Transfer Level Synthesis: From Theory to Practice", IEEE International Conference on VLSI Design, January 1996
- "A Survey of Optimization Techniques Targeting Low Power VLSI Circuits", ACM Design Automation Conference, June 1995
- "Embedded Systems Performance Analysis", IEEE International Conference on Computer Design, October 1993
- "Multi-level Logic Synthesis", IEEE International Conference on Computer-Aided Design, November 1991, November 1992
- "Sequential Logic Synthesis", IEEE International Conference on VLSI Design, January 1991

Publications

Books

- Computer Aided Verification, 20th International Conference, CAV 2008, Princeton, NJ, USA, July 7-14, 2008, Proceedings. Lecture Notes in Computer Science 5123 Springer 2008, ISBN 978-3-540-70543-7 (Edited Volume, co-edited with A. Gupta)
- Performance Analysis of Real-Time Embedded Software, (with Yau-Tsun Steven Li), Kluwer Academic Publishers, 1999.

Book Chapters

- Conflict-driven clause learning SAT solvers, (with J Marques-Silva, I Lynce) in Handbook of satisfiability, Pages 133-182, ios Press, 2021
- Post-Silicon Fault Localization with Satisfiability Solvers. (with G. Weissenbacher) In: Mishra P., Farahmandi F. (eds) Post-Silicon Validation and Debug. Springer, Cham, 2019
- Propositional SAT Solving, in Handbook of Model Checking (with J. Marques-Silva) 2018: 247-275
- Verifying Security Properties in Modern SoCs using Instruction Level Abstractions, in Hardware IP Security and Trust, (with P. Subramanyan), Editors: P. Mishra, S. Bhunia, M. Tehranipoor, Springer, 2017

- Boolean Satisfiability: Solvers and Extensions, in Software Systems Security, (with G. Weissenbacher and P. Subramanyan), Editors: O. Grumberg, H. Seidl, M. Irlbeck, Publisher: IOS Press, NATO Science for Peace and Security Series, 2014
- Boolean Satisfiability Solvers: Techniques and Extensions, in Tools for Analysis and Verification of Software Safety and Security, (with G. Weissenbacher), Editors: T. Nipkow, O. Grumberg, B. Hauptmann, G. Kalus, Publisher: IOS Press, NATO Science for Peace and Security Series, Spring 2012
- Conflict-Driven Clause Learning, SAT Solvers, in Handbook of Satisfiability, (with J. Marques-Silva and I. Lynce), Edited by A. Biere, H. van Maaren, and T. Walsh, Production editor M. Heule, IOS Press, 2008
- MADL: An ADL based on a Formal and Flexible Concurrency Model, in Processor Description Languages: Applications and Methodologies, Morgan Kaufman Publishers, (with W. Qin, S. Rajagopalan), Morgan Kaufman, P. Mishra, N. Dutt, Editors, 2008
- Architecture Description Languages for Retargetable Compilation, (with W. Qin), in The Compiler Design Handbook: Optimizations & Machine Code Generation, CRC Press, Second Edition 2007, Y. N. Srikant and Priti Shankar, Editors
- A Retargetable VLIW Compiler Framework for DSPs, (with S. Rajagopalan), in The Compiler Design Handbook: Optimizations & Machine Code Generation, CRC Press, Second Edition, 2007, Y. N. Srikant and Priti Shankar, Editors
- Boolean Satisfiability: Creating Solvers Optimized for Specific Problem Instances, (with P. Zhong and M. Martonosi), Reconfigurable Computing: The Theory and Practice of FPGA Computation, Editors: S. Hauck and A. DeHon, Elsevier Publishers, 2007
- A Case for Runtime Validation of Hardware, Hardware and Software, Verification and Testing: First International Haifa Verification Conference, Haifa, Israel, November 13-16, 2005, Revised Selected Papers, Lecture Notes in Computer Science, Springer Volume 3875/2006, Editors: S. Ur, E. Bin, Y. Wolfsthal
- ZChaff2004: An Efficient SAT Solver, (with Y.Mahajan, Z. Fu), Theory and Applications of Satisfiability Testing, 7th International Conference, SAT 2004. Selected Revised Papers Series: Lecture Notes in Computer Science
- Analysis of Search Based Algorithms for Satisfiability of Quantified Boolean Formulas Arising from Circuit State Space Diameter Problems, (with D. Tang, Y. Yu and D. Ranjan), Theory and Applications of Satisfiability Testing, 7th International Conference, SAT 2004. Selected Revised Papers Series: Lecture Notes in Computer Science
- Cache Performance of SAT Solvers: A Case Study for Efficient Implementation of Algorithms," (with L. Zhang), Theory and Applications of Satisfiability Testing, 6th International Conference, SAT 2003. Santa Margherita Ligure, Italy, May 5-8, 2003 Selected Revised Papers Series: Lecture Notes in Computer Science, Vol. 2919, 2004, Giunchiglia, E.; Tacchella, A. (Eds.)
- Modeling and Integration of Peripheral Devices in Embedded Systems, (with S. Wang and R. A. Bergamaschi), in Embedded Software for SoC, Kluwer Academic Publishers, 2003, A. Jerraya, S. Yoo, N. Wehn, and D. Verkest, Editors
- SAT and ATPG: Algorithms for Boolean Decision Problems, (with W. Kunz and J. Marques-Silva), in Logic Synthesis and Verification, Kluwer Academic Publishers, 2001, S. Hassoun and T. Sasao, Editors
- Instruction Level Power Analysis and Optimization of Software, (with V. Tiwari, A. Wolfe and M. T-C. Lee), in Technologies for Wireless Computing, Kluwer Academic Publishers, 1996, A. P. Chandrakasan and R. W. Brodersen, Editors
- Code Generation and Optimization Techniques for Embedded Digital Signal Processors, (with S. Liao, S. Devadas, K. Keutzer, S. Tjiang, A. Wang, G. Araujo, A. Sudarsanam, V. Ziviojnovic, H. Meyr) in Hardware Software Codesign, Kluwer Academic Publishers, NATO-ASI Series, 1996, G. DeMicheli and M. Sami, Editors

- Performance Analysis of Embedded Systems, (with W. Wolf, A. Wolfe, Y-T S. Li, T-Y Yen), in Hardware Software Codesign, Kluwer Academic Publishers, NATO-ASI Series, 1996, G. DeMicheli and M. Sami, Editors
- Challenges in Code Generation for Embedded Processors (with G. Araujo, S. Devadas, K. Keutzer, S. Liao, A. Sudarsanam, S. Tjiang, A. Wang) in Code Generation for Embedded Processors, Kluwer Academic Publishers, 1995, P. Marwedel and G. Goossens, Editors

Refereed Journal and Conference Papers

1. "CNNFlow: Memory-Driven Data Flow Optimization for Convolutional Neural Networks," (with Q. Nie), Transactions on Design Automation of Electronic Systems (ACM TODAES), accepted for publication.
2. "Compositional Verification Using a Formal Component and Interface Specification," (with Y. Xing, H. Lu and A. Gupta), IEEE/ACM International Conference on Computer-Aided Design, ICCAD 2022.
3. "Usage-Based RTL Subsetting for Hardware Accelerators," (with Q. Tan and A. Gupta), IEEE/ACM International Conference on Computer-Aided Design, ICCAD 2022.
4. "ADA, the Center for Applications Driving Architectures: Accomplishments and Vision Forward (with V. Bertacco, T. Austin, D. Brooks, Z. Tatlock, G-Y Wei, T F. Wenisch), Design Automation Conference, DAC 2022.
5. "Automatic Generation of Architecture-Level Models from RTL Designs for Processors and Accelerators," (with Y. Zeng and A. Gupta), Design, Automation and Test in Europe Conference, DATE 2022
6. "Generalizing Tandem Simulation: Connecting High-level and RTL Simulation Models," (with Y. Xing and A. Gupta), 27th Asia and South Pacific Design Automation Conference, ASP-DAC 2022
7. "Software-Driven Security Attacks: From Vulnerability Sources to Durable Hardware Defenses," Lauren Biernacki, Mark Gallagher, Zhixing Xu, Misiker Tadesse Aga, Austin Harris, Shijia Wei, Mohit Tiwari, Baris Kasikci, Sharad Malik, Todd Austin, ACM Journal on Emerging Technologies in Computing Systems, Volume 17, Issue 3, August 2021
8. "Leveraging Processor Modeling and Verification for General Hardware Modules" (with Yue Xing, Huaixi Lu, and Aarti Gupta), Design, Automation & Test in Europe Conference (DATE), 2021
9. "Syntax-Guided Synthesis for Lemma Generation in Hardware Model Checking" (with H. Zhang and A. Gupta), 22nd International Conference on Verification, Model Checking, and Abstract Interpretation, 2021
10. "Generating Architecture-Level Abstractions from RTL Designs for Processors and Accelerators Part I: Determining Architectural State Variables, (with Y Zeng, BY Huang, H Zhang, A Gupta), 2021 IEEE/ACM International Conference On Computer Aided Design (ICCAD)
11. "MemFlow: Memory-Driven Data Scheduling With Datapath Co-Design in Accelerators for Large-Scale Inference Applications," (with Q.Nie) in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 39, no. 9, pp. 1875-1888, Sept. 2020, doi: 10.1109/TCAD.2019.2925377.
12. "Synthesizing Environment Invariants for Modular Hardware Verification," (with H. Zhang, W. Yang, G. Fedyukovich and A. Gupta), 21st International Conference on Verification, Model Checking, and Abstract Interpretation, 2020

13. “Sparse Matrix to Matrix Multiplication: A Representation and Architecture for Acceleration,” (with. A. Golnari), The 30th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP) 2019
14. “Revealing Cluster Hierarchy in Gate-level ICs Using Block Diagrams and Cluster Estimates of Circuit Embedding,” (with B. Cakir), ACM Transactions on Design Automation of Electronic Systems (TODAES), 24(5): 50:1-50:19, 2019
15. “Instruction-Level Abstraction (ILA): A Uniform Specification for System-on-Chip (SoC) Verification,” (with B-Y. Huang, H. Zhang, P. Subramanyan, Y. Vizel, and A. Gupta), ACM Transactions on Design Automation of Electronic Systems (TODAES), 24(1): 10:1-10:24, 2019
16. “ILAng: A Modeling Platform for SoC Verification using Instruction-Level Abstractions,” (with B-Y. Huang, H. Zhang, and A. Gupta), 25th International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS), 2019
17. “SpFlow: Memory-Driven Data Flow Optimization for Sparse Matrix-Matrix Multiplication,” (with Q. Nie), IEEE International Symposium on Circuits and Systems, 2019
18. “Morpheus: A Vulnerability-Tolerant Secure Architecture Based on Ensembles of Moving Target Defenses with Churn,” (with M. Gallagher, L. Biernacki, S. Chen, Z. B. Aweke, S. F. Yitbarek, M. T. Aga, A. Harris, Z. Xu, B. Kasikci, V. Bertacco, M. Tiwari, T. Austin, 24th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS '19), 2019
19. “A Formal Instruction-Level GPU Model for Scalable Verification,” (with Y. Xing, B-Y Huang, and A. Gupta), IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2018
20. (Invited Paper) “Vulnerability-Tolerant Secure Architectures,” (with T. Austin, V. Bertacco, B. Kasikci, and M. Tiwari), IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2018
21. “ Integrating Memory Consistency Models with Instruction-Level Abstraction for Heterogeneous System-on-Chip Verification,” with H. Zhang, C. Trippel, Y Manerkar, A. Gupta, and M Martonosi, Formal Methods in Computer-Aided Design (FMCAD), 2018
22. “Lazy Self-Composition for Security Verification,” with W. Yang, P. Subramanyan, Y. Vizel and A. Gupta, International Conference on Computer-Aided Verification (CAV), 2018
23. “Reverse Engineering Digital ICs Through Geometric Embedding of Circuit Graphs,” with B. Cakir, ACM Transactions on Design Automation of Electronic Systems (TODAES), TODAES, Volume 23 Issue 4, July 2018
24. “Formal Security Verification of Concurrent Firmware in SoCs using Instruction-Level Abstraction for Hardware,” with B-Y. Huang, J. Fung, S. Ray and A. Gupta, ACM/IEEE Design Automation Conference (DAC) 2018
25. “MemFlow: Memory-Driven Data Scheduling with Datapath Co-design in Accelerators for Large-Scale Inference Applications,” with Q. Nie, ACM/IEEE 23rd Asia and South Pacific Design Automation Conference (ASP-DAC) 2018
26. “Template-based Parameterized Synthesis of Uniform Instruction-Level Abstractions for SoC Verification,” with P. Subramanyan, B-Y. Huang, Y Vizel and A. Gupta, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017
27. “Trace-based Analysis of Memory Corruption Malware Attacks,” with Z. Xu and A. Gupta, Thirteenth Haifa Verification Conference (HVC), 2017
28. “Solving Linear Arithmetic with SAT-based Model Checking,” with Y Vizel and A. Nadel, Formal Methods in Computer-Aided Design (FMCAD), 2017

29. “PPU: A Control Error-Tolerant Processor for Streaming Applications with Formal Guarantees,” with A. Golnari, Y. Yetim, Y. Vizel and M. Martonosi, ACM Journal on Emerging Technologies in Computing Systems, Special Issue on Alternative Computing Systems, Volume 13, Issue 3, 2017.
30. “IC3 - Flipping the E in ICE,” with Y. Vizel, A. Gurfinkel, S. Shoham, 18th International Conference on Verification, Model Checking, and Abstract Interpretation (VMCAI), 2017.
31. “Malware Detection using Machine Learning Based Analysis of Virtual Memory Access Patterns,” with Z. Xu, S. Ray and P. Subramanyan, Design, Automation & Test in Europe Conference (DATE), 2017.
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